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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,509	07/28/2003	Fang-Yu Yeh	10380-US-PA	1508

31561 7590 11/19/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
DANG, PHUC T	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,509	YEH ET AL.	
	Examiner	Art Unit	
	PHUC T DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *election filed on October 7, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *021304*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election filed on October 7, 2004 has been considered.

In election, Applicants elect Group I (claims 1-14) without traverse and cancel Group II (claims 15-23).

Claims 1-14 are currently pending in the application.

Oath/Declaration

2. The oath/declaration filed on July 28, 2003 is acceptable.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on February 13, 2004.

Specification

5. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (U.S. Patent No. 5,677,228) in view of Nam (U.S. Patent No. 6,765,252).

Tseng discloses a method of manufacturing a semiconductor device, comprising: the steps of:

providing a substrate (30, Fig. 3);

forming a mask layer (38, Fig. 3) over the substrate;

patterning the mask layer (38, Fig. 4) and the substrate (30, Fig. 4) to form a first opening (40, Fig. 4) in the substrate;

forming a gate dielectric layer (42, Fig. 5),a first conductive layer (44, Fig. 5) and a second conductive layer (46, Fig. 5) inside the first opening sequentially, wherein the gate dielectric layer covers the interior surface of the first opening, the first conductive layer covers the gate dielectric layer and the second conductive layer completely fills the first opening;

removing a portion of the first conductive layer (44, Fig. 7) and the second conductive layer (46, Fig. 7) so that the upper surface of a remaining first conductive layer and a remaining second conductive layer in the opening are at a level slightly below the upper surface of the substrate and thereby form a second opening.

Tseng discloses all the features of the claimed invention as discussed above, but doest not disclose a step of forming a cap layer inside the second opening; removing the mask layer; and forming a source/drain region in the substrate.

Nam; however, discloses a step of forming a cap layer (45, Fig. 8) inside the second opening; removing the mask layer (46, Fig. 8); and forming a source/drain region (41, Fig. 9) in the substrate.

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Nam to Tseng discussed above such that a step of forming a cap layer inside the second opening, removing the mask layer and forming a source/drain region in the substrate for a purpose of improving a manufacturing of a semiconductor device.

Regarding claims 2-6, Nam discloses the steps of forming the source/drain region relating to the implanting mask layer and location of the well region is formed in the substrate.

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Nam to Tseng discussed above such that the steps of forming the source/drain region as disclosed in claims 2-6 for a purpose of improving a manufacturing of a semiconductor device.

Regarding claim 8, Tseng discloses the first conductive layer comprises a polysilicon layer [col. 3, lines 6-13].

Regarding claims 11-12, Tseng discloses the step of removing and the second

a portion of the first conductive layer conductive layer comprises performing a chemical-mechanical polishing process to remove portions of the first conductive layer and the second conductive layer outside the opening, and etching back the first conductive layer and the second conductive layer in the opening so that the upper surface of the remaining first conductive layer and the remaining second conductive layer in the opening are at a level slightly below the upper surface of the substrate and thereby form a second opening and the mask layer is fabricated using a material having an etching selectivity that differs from the material constituting the first conductive layer, the second conductive layer and the cap layer [Fig. 2B and col. 1, lines 36-53].

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng and Nam in view of Liu et al., hereafter "Liu" (U.S. Patent No. 6,509,249).

Tseng and Nam disclose all the features of the claimed invention as discussed above, but do not disclose wherein after the step of forming a mask layer over the substrate, furthermore comprises forming a bottom anti-reflection layer over the mask layer, and the step of patterning the mask layer a first opening furthermore and the substrate to form comprises patterning the bottom anti-reflection layer.

Liu, however, discloses wherein after the step of forming a mask layer over the substrate, furthermore comprises forming a bottom anti-reflection layer over the mask layer, and the step of patterning the mask layer a first opening furthermore and the substrate to form comprises patterning the bottom anti-reflection layer [Fig. 1C].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Nam and Tseng to Liu discussed above such that wherein after the step of forming a mask layer over the substrate, furthermore comprises forming a bottom anti-reflection layer over the mask layer, and the step of patterning the mask layer a first opening furthermore and the substrate to form comprises patterning the bottom anti-reflection layer for a purpose of improving a manufacturing of a semiconductor device.

8. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng and Nam in view of Liu et al., hereafter "Liu" (U.S. Patent No. 6,046,108).

Tseng and Nam disclose all the features of the claimed invention as discussed above, but do not disclose wherein the second conductive layer comprises a refractory metal silicide layer. and wherein material constituting the refractory metal silicide layer is selected from a group consisting of tungsten silicide, nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, platinum silicide and palladium silicide.

Liu, however, discloses wherein the second conductive layer comprises a refractory metal silicide layer and wherein material constituting the refractory metal silicide layer is selected from a group consisting of tungsten silicide, nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, platinum silicide and palladium silicide [Fig. 1A and col. 4, lines 19-23].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Nam and Tseng to Liu discussed above such that the material of the conductive is selected as disclosed in claims 9-10 for a purpose of improving a manufacturing of a semiconductor device.

Allowable Subject Matter

9. Claims 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

None of the Prior art of record disclose wherein after the step of mask layer and the substrate to form the comprises performing a threshold voltage adjustment process as recited in claim 13 and a step of forming an inter-layer dielectric and layer over the substrate, forming a contact opening in the inter-layer dielectric layer using the cap layer as a self-aligned mask as recited in claim 14.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and After Final communications.

12. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

PD

Phuc T. Dang

Primary Examiner

Art Unit 2818